PVP 14

Code: EC3T6, EE3T6

II B.Tech - I Semester – Regular/Supplementary Examinations
November 2019

SWITCHING THEORY AND LOGIC DESIGN

(Common for ECE, EEE)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) What is the largest binary number that can be expressed with

   i) 14-bits ii) 10-bits

b) Find 16's compliment of BABA.

c) Reduce the Boolean function (A′+C)(A′+C′)(A+B+CD) to four literals.

d) Draw the logic diagram to implement the function Y=(A′+B′)(C+D′)

e) Distinguish between combinational and sequential switching circuits.

f) Draw the logic diagram of four-to-one line multiplexer.

g) Draw the logic diagram of 4x2 encoder.

h) Convert JK flip- flop to D flip- flop.

i) Draw the logic diagram of a mod-7 asynchronous counter using JK flip-flops.

j) What are the various types of shift registers?

k) Compare the Moore and Mealy Machines.

PART – B

Answer any ***THREE*** questions. All questions carry equal marks. 3 x 16 = 48 M

2. a) Convert the following to Decimal and then to Binary.

i) $(3214)_{16}$ ii) $(2716)_{8}$ 8 M

b) Explain about different Error Correction and Detection codes. 8 M

3. a) Express the following function as a sum of min terms and as a product of max terms.

$F(A,B,C,D) = B'D + A'D + BD$ 8 M

b) Simplify the following Boolean function together with don't care conditions d, and implement it using NAND gates. 8 M

$F(A,B,C,D) = \sum m(0,6,8,13,14) + \sum d(2,4,10)$

4. a) Design a 4 bit adder-subtractor and explain its operation. 8 M

b) Draw a PLA circuit to implement the functions. 8 M

$F_1 = A'B + AC' + A'BC'$

$F_2 = (AC + AB + BC)'$

5. a) Design a 4 bit synchronous counter using JK Flip-flops and explain its operation. 8 M

b) Draw the logic diagram of a 4-bit up-down ripple counter and explain its operation. 8 M

6. a) A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip – flop input equations and circuit output equation are 8 M

$J_A = Bx + B'y'$ $K_A = B' xy'$

$J_B = A'x$ $K_B = A+xy'$

$z = Ax'y' + Bx'y'$

i) Draw the logic diagram of the circuit.

ii) Tabulate the state table

iii) Derive the state equations for A and B.

b) Reduce the number of states in the following state diagram and design the circuit using T Flip-flops. 8 M